

Annual Course Report

(LOGIC DESIGN-1)

A-Basic Information

- Title and Code
 Programme(s) on which this course is given
 CS, IS, OR and IT
- **3-** Academic year / Level of programme
 1st year -2nd Semester
- 4- Units/Weekly hours

Lecture 3 Tutorial/Practical 3 Total 6

5- Names of lecturers contributing to the delivery of the course

1- Prof. Fawzy Ali Torkey

Course co-ordinator: Prof. Fawzy Ali Torkey External evaluators: Not assigned yet.

B- Statistical Information



C-Professional Information

1- Course Teaching

	Topics actually taught	No. of hours	Lecturer
1	Introduction	3	Prof. Fawzy Ali Torkey
2	 Number systems and Codes Binary, Octal and Hex Number Systems Number Systems Conversions. BCD, Gray and Alphanumeric Codes. Error Detection. 	12	Prof. Fawzy Ali Torkey
3	 Digital Arithmetic Binary addition and Subtraction. Binary Multiplication and Division. BCD Addition and Hex. Arithmetic 	6	Prof. Fawzy Ali Torkey
4	 Logic Gates Boolean Constants and Variables. Truth Tables. OR, AND, and NOT Operations. Logic Algebra and Logic Implementation. NOR and NAND Gates. 	9	Prof. Fawzy Ali Torkey
5	 Boolean Algebra and Logic Simplification Boolean and Demorgan's Theorems. Universality of NAND and NOR Gates. Alternative Representations. Labeling Logic Signals. SOP and POS Forms. Simplifying Logic Circuits using algebra and K-maps. 	15	Prof. Fawzy Ali Torkey
6	 Combinational Logic Introduction Basic Circuits and Design Procedure. Using NAN and NOR gates in Design. Display Devices 	6	Prof. Fawzy Ali Torkey
7	 Programmable Logic Introduction Programmable arrays Programmable Array logic Generic Array Logic The GALs 22V10 and 16V8 Introduction to CPLDs and FPGAs 	6	Prof. Fawzy Ali Torkey

 8 Combinational Circuits Introduction. Arithmetic Circuits and Comparators. Decoders and Encoders. Multiplexers and Demultiplexers. 	12	Prof. Fawzy Ali Torkey
 9 Combinational Logic Programming. Introduction Describing Logic circuits Development Software Description languages and Programming Languages Implementing Logic Circuits using PLDs VHDL Format and Syntax Intermediate signals in VHDL Representing Data in VHDL Truth Tables using VHDL Decision Control Structures Implementing Adders, Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators, Code Converters. 	12	Prof. Fawzy Ali Torkey
 10 Logic Families Introduction. Diode, RTL, DTL, ECL, and TTL Logic. CMOS Logic. 	3	Prof. Fawzy Ali Torkey

Topics taught as a percentage of the content specified:

	• •
>90	%
	, .

70-90 %

<70%

2- Teaching and Learning Methods:

 \checkmark

Lectures:√Practical Training/ Laboratory:√Seminar/Workshop:√Class Activity:√Case Study:√Other Assignments/Homework:√

3- Student Assessment:

Method of Assessment	Percentage of total
Written examination	60
Oral examination	10
Practical/laboratory work	10
Other Assignments/class work	20
Total	100 %

Members of Examination Committee: Prof. Fawzy Ali Torkey Mr. Abd El-Alem Kamal

Role of external evaluator: External evaluator not assigned yet.

4- Facilities and Teaching Materials:

Totally adequate	
Adequate to some extent	\checkmark
Inadequate	

5- Administrative Constraints

•Period time of Practical Training /laboratory per week not enough.

- Needing a maintenance team for Logic Laboratory.
- Needing more funds for more devices needed by course co-ordinator.

6- Student Evaluation of the course: Response of Course Team

Need more time to execute their exercises in lab

Talking with administration to increase time for staying students in lab.

7- Comments from external evaluator(s):

External evaluator not assigned yet.

8- Course Enhancement:

Progress on actions identified in the previous year's action plan: No previous years action plan

Role of external evaluator:

External evaluator not assigned yet

9- Action Plan for Academic Year 2006 – 2007

Actions RequiredCompletion DatePerson ResponsibleGet more FPGA boards
for student to implement
cryptography algorithms
on it.2008Prof. fawzy ali Torkey

Course Coordinator: Prof. fawzy ali Torkey

Signature:

Date / /